IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:		TI-33763
	Song Wu, et al.	Art Unit: 2611
Serial No:	10/603,302	Examiner: Jaison Joseph
Filed:	June 25, 2003	Conf. No.: 5280
For:	Decision Feedback Equalization for High Speed Serial Links	

Appeal Brief Under 37 C.F.R. §41.37

Board of Patent Appeals and Interferences
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is Appellant's Appeal Brief filed pursuant to 37 C.F.R. §41.37 in connection with the above-identified application in response to the Final Rejection mailed March 21, 2007, and the Notice of Appeal mailed by Applicant on July 23, 2007.

Real Party in Interest

The real party in interest in this application is Texas Instruments Incorporated, a corporation of Delaware with its principle place of business in Dallas, Texas. An assignment to Texas Instruments Incorporated is recorded at reel 013275 and frame 0196 to 0198.

Related Appeals and Interferences

There are no appeals of interferences related to this appeal in this application.

Status of the Claims

Claims 1-25 are the subject of this appeal. Claims 1-25 are rejected. This application was filed on June 25, 2003.

Status of Amendments Filed After Final Rejection

The Appellants filed an amendment under 37 C.F.R. § 1.116 on June 14, 2007 in response to the Office Action dated March 21, 2007, with no amendments to the claims.

Summary of Claimed Subject Matter

Claim 1:

Specification page 11, line 3 to page 12, line 8, provides a concise explanation of the invention defined in claim 1.

The input for receiving in Claim 1 is the input to AGC in Figure 1.

The feedforward equalizer in Claim 1 is wire summation node 15 in Figure 1.

The sampler in Claim 1 is Sampler 13 in Figure 1.

The feedback equalizer in Claim 1 includes the DACs and delay elements D in Figure 1.

Exemplary embodiments of a receiver DFE implementation according to the invention are shown in FIGURE 1. An analog AGC (automatic gain control) block buffers the analog input to prevent the feedback signal $s(t)$ from echoing back to the line. The buffered analog input signal $y(t)$, in this example current, is wire summed with the synthesized signal $s(t)$. The sampling receiver 13 takes samples from the mixed signal $z(t)$ to make the symbol decision. The decision symbols are then fed back to construct the new feedback signal $s(t)$. As shown in FIGURE 1, the decision symbols S_k (k = 1, … K) at different delay stages drive respective current source digital to analog converters (DAC) which are controlled by weights dfe_k (k = 1, … K) that define the taps of feedback signal $s(t)$.

In some embodiments, the tap weights dfe_k are real numbers in 2's complement format. Assuming, for example, that each weight dfe_k includes B bits which represent the magnitude of dfe_k, plus an additional bit to represent the sign of dfe_k, then for each of the K taps, the associated DAC has B parallel-connected current switch transistors. In some embodiments of FIGURE 1A, the B magnitude bits of dfe_k are thermometer-coded, and each of the resulting B thermometer-coded bits controls a respectively corresponding one of the B transistor switches. Each decision symbol S_k includes complementary bits s_k and $\overline{s_k}$ which are combined (e.g. multiplied) with the associated sign bit as shown in FIGURE 1A to control the polarity of the current that the corresponding DAC contributes to the wire summation node 15. Node 15 thus functions as a feedforward equalizer.

The receiver sampler and each delay stage are triggered by the symbol clock (not explicitly shown), so the $s(t)$ waveform is a square wave with each pulse having one-symbol duration T. The leading tap is time critical, so some embodiments require the circuit delay from the decision sampler 13 to the leading tap DAC output to be less than half of the symbol period.

Claim 13:

Specification page 12, line 11 to page 12, line 16, provides a concise explanation of the invention defined in claim 13.

The input for receiving in Claim 13 is the input to the DACs in Figure 2.

The digital-to-analog conversion portion in Claim 13 includes the DACS in Figure 2.

The output coupled to said digital-to-analog conversion portion in Claim 13 is the Transmitter Output in Figure 2.

The control input for receiving control information in Claim 13 is the Programmable Coefficients in Figure 2.

Referring again to the above-described transmitter pre-emphasis implementation, exemplary embodiments thereof are shown in FIGURE 2. Similar to the filter structure in FIGURE 1, each pre-emphasis tap weight c_k (k = 0, 1 … K – 1), which can be a real number in 2's complement format, controls the magnitude of a current source DAC, and the incoming data is combined with the sign bit of c_k to control the polarity flowing through the wire summation node. The filter coefficients are determined by the solution of Equation (7).

Equation 7

$$\sum_n c_n \cdot \varphi(t_{\max} - nT - T/2) \cdot \delta_{k,1} - \sum_n (c_n + c_{n+1}) \cdot \varphi(t_{\max} + kT - nT - T/2) + \sum_n (c_{n-1} + 2 \cdot c_n + c_{n+1}) \cdot \varphi(t_{\max} + kT - nT)/2 = 0$$

Claim 17:

Specification page 11, line 3 to page 12, line 8, provides a concise explanation of the invention defined in claim 17.

The input for receiving in Claim 17 is the input to the AGC in Figure 1.

The output for providing in Claim 17 is the output of the Sampler in Figure 1.

The equalizer in Claim 17 includes the summation node 15 and the DACs in Figure 1.

The equalizer coefficient in Claim 17 is dfe1, dfe2, and dfek in Figure 1.

The coefficient adaptor apparatus in Claim 17 is the Training block in Figure 1 and thermometer coding block in Figure 1A.

Exemplary embodiments of a receiver DFE implementation according to the invention are shown in FIGURE 1. An analog AGC (automatic gain control) block buffers the analog input to prevent the feedback signal $s(t)$ from echoing back to the line. The buffered analog input signal $y(t)$, in this example current, is wire summed with the synthesized signal $s(t)$. The sampling receiver 13 takes samples from the mixed signal $z(t)$ to make the symbol decision. The decision symbols are then fed back to construct the new feedback signal $s(t)$. As shown in FIGURE 1, the decision symbols S_k (k = 1, … K) at different delay stages drive respective current source digital to analog converters (DAC) which are controlled by weights dfe_k (k = 1, … K) that define the taps of feedback signal $s(t)$.

In some embodiments, the tap weights dfe_k are real numbers in 2's complement format. Assuming, for example, that each weight dfe_k includes B bits which represent the magnitude of dfe_k, plus an additional bit to represent the sign of dfe_k, then for each of the K taps, the associated DAC has B parallel-connected current switch transistors. In some embodiments of

FIGURE 1A, the B magnitude bits of dfe_k are thermometer-coded, and each of the resulting B thermometer-coded bits controls a respectively corresponding one of the B transistor switches. Each decision symbol S_k includes complementary bits s_k and $\overline{s_k}$ which are combined (e.g. multiplied) with the associated sign bit as shown in FIGURE 1A to control the polarity of the current that the corresponding DAC contributes to the wire summation node 15. Node 15 thus functions as a feedforward equalizer.

The receiver sampler and each delay stage are triggered by the symbol clock (not explicitly shown), so the $s(t)$ waveform is a square wave with each pulse having one-symbol duration T. The leading tap is time critical, so some embodiments require the circuit delay from the decision sampler 13 to the leading tap DAC output to be less than half of the symbol period.

Claim 23:

Specification page 7, line 12 to page 12, line 8, provides a concise explanation of the invention defined in claim 23.

Exemplary embodiments of the present invention as illustrated in FIGURE 1 can widen the eye. As shown in FIGURE 1, a correction waveform s(t) can be synthesized at the receiver front end and mixed with the incoming waveform y(t) before the data is taken. Mathematically the synthesized correction waveform is

$$s(t) = -\sum_{k=1} dfe_k \cdot a_{m-k} \cdot u(t-(m-1)T-\Delta),$$

where $u(t)$ is a unit rectangle function with width T, and Δ is implementation delay such that $\Delta = T/2$, dfe_k are filter coefficients obtained with channel response and a_{m-k} are previously decoded data. The effective signal strength $z(t) = y(t) + s(t)$ at the eye open point $t = mT + t_{\max}$ is

$$z_m = a_m \cdot \varphi(t_{\max}) + \sum_{i=-I}^{-1} a_{m+i} \cdot \varphi(t_{\max} - iT) + \sum_{k=0\cdots} a_{m-1-k} \cdot \varphi(t_{\max} + T + kT) - \sum_{k=0} \hat{a}_{m-1-k} \cdot dfe_{k+1},$$

and at the crossing point $t = mT + t_{\max} - T/2$ is

$$z_{m-1/2} = \sum_{k=0\cdots} a_{m-1-k} \cdot \varphi(t_{\max} + T/2 + kT) + a_m \cdot \varphi(t_{\max} - T/2) + \sum_{i=-I}^{-1} a_{m+i} \cdot \varphi(t_{\max} - iT)$$
$$- \sum_{k=0\cdots} dfe_{k+1} \cdot (\hat{a}_{m-1-k} + \hat{a}_{m-2-k})/2$$

In the foregoing effective signal strength equations, "$\hat{a}$" represents the decoded version of the corresponding transmitted symbol "a".

At the receiver dfe_k and $t_{\max}$ are chosen so that $E\{z_{m-1/2}^2\} \to 0$ when $a_m = -a_{m-1}$ to achieve minimum jitter. Since a_{m-k}, with $k > 1$ are independent variables, we can rearrange above equation as

$$z_{m-1/2} = \sum_{k=0\cdots} a_{m-1-k} \cdot \varphi(t_{\max} + T/2 + kT) + a_m \cdot \varphi(t_{\max} - T/2) + \sum_{i=-I}^{-1} a_{m+i} \cdot \varphi(t_{\max} - T/2 - iT)$$
$$- \sum_{k=0\cdots} dfe_{k+1} \cdot (\hat{a}_{m-1-k} + \hat{a}_{m-2-k})/2$$
$$= a_m \cdot \varphi(t_{\max} - T/2) + \sum_{i=-I}^{-1} a_{m+i} \cdot \varphi(t_{\max} - T/2 - iT)$$
$$+ \sum_{k=0\cdots} a_{m-1-k} \cdot \{\varphi(t_{\max} + T/2 + kT) - (def_{k+1} + dfe_k)/2\}$$

and,

$$E\{z_{m-1/2}^2\} = \varphi(t_{\max} - T/2)^2 + \sum_{k=0\cdots} \{\varphi(t_{\max} + T/2 + kT) - (def_{k+1} + dfe_k)/2\}^2$$
$$- 2 \cdot \varphi(t_{\max} - T/2) \cdot \{\varphi(t_{\max} + T/2) - dfe_1/2\} + \sum_{i=-I}^{-1} \varphi(t_{\max} - T/2 - iT)^2$$
$$= \{\varphi(t_{\max} - T/2) - \varphi(t_{\max} + T/2) + dfe_1/2\}^2 + \sum_{k=0\cdots} \{\varphi(t_{\max} + T/2 + kT) - (def_{k+1} + dfe_k)/2\}^2$$
$$+ \sum_{i=-I}^{-1} \varphi(t_{\max} - T/2 - iT)^2$$

T

he dfe_k is available by making $\frac{\partial E\{z_{m-1/2}^2\}}{\partial dfe_k} = 0$.

Equation 5

$$\varphi(t_{\max} - T/2)\cdot\delta_{k,1} - \varphi(t_{\max} - T/2 + kT) - \varphi(t_{\max} + T/2 + kT) + (dfe_{k-1} + 2\cdot dfe_k + dfe_{k+1})/2 = 0$$

As an example of four dfe taps, four equations are available to guarantee unique solution.

$$with\, k=1:\ \{\varphi(t_{\max} - T/2) - \varphi(t_{\max} + T/2)\} - \varphi(t_{\max} + 3T/2) + (2\cdot dfe_1 + dfe_2)/2 = 0$$
$$with\, k=2:\ -\varphi(t_{\max} + 3T/2) - \varphi(t_{\max} + 5T/2) + (dfe_1 + 2\cdot dfe_2 + dfe_3)/2 = 0$$
$$with\, k=3:\ -\varphi(t_{\max} + 5T/2) - \varphi(t_{\max} + 7T/2) + (dfe_2 + 2\cdot dfe_3 + dfe_4)/2 = 0$$
$$with\, k=4:\ -\varphi(t_{\max} + 7T/2) - \varphi(t_{\max} + 9T/2) + (dfe_3 + 2\cdot dfe_4)/2 = 0$$

At the eye open point, the effective signal strength equation can be rearranged as

$$z_m = a_m\cdot\varphi(t_{\max}) + \sum_{i=-I}^{-1} a_{m+i}\cdot\varphi(t_{\max} - iT) + \sum_{k=0\cdots} a_{m-1-k}\cdot\varphi(t_{\max} + T + kT) - \sum_{k=0}\hat{a}_{m-1-k}\cdot dfe_{k+1}$$
$$= a_m\cdot\varphi(t_{\max}) + \sum_{i=-I}^{-1} a_{m+i}\cdot\varphi(t_{\max} - iT) + \sum_{k=0\cdots} a_{m-1-k}\cdot\{\varphi(t_{\max} + T + kT) - dfe_{k+1}\}$$

in which the first term is proportional to the signal strength, and the second term is the residual ISI. The power of residual ISI can be estimated by

$E\{isi^2\} = \sum_{i=-I}^{-1}\varphi(t_{\max} - iT)^2 + \sum_{k=0\cdots}\{\varphi(t_{\max} + T + kT) - dfe_{k+1}\}^2$. By minimizing the residual ISI, i.e., making $\frac{\partial E\{isi^2\}}{\partial dfe_k} = 0$, second set of equations is available

Equation 6

$$\varphi(t_{\max} + kT) = dfe_k$$

In general Equations (5) and (6) can not be satisfied at the same time. However, using a transmitter pre-emphasis technique as shown in FIGURE 2, the transmitter pulse becomes $P(t) = \sum_n c_n\cdot p(t - nT)$. The new aggregate channel response is then $\varphi'(t) = \sum_n c_n\cdot\varphi(t - nT)$, and should satisfy Equations (5) and (6) at the same time. Substituting $\varphi'(t)$ for $\varphi(t)$ in Equations 5 and 6, and combining Equations 5 and 6, the solution of c_n is given by

Equation 7

$$\sum_n c_n \cdot \varphi(t_{\max} - nT - T/2) \cdot \delta_{k,1} - \sum_n (c_n + c_{n+1}) \cdot \varphi(t_{\max} + kT - nT - T/2) + \sum_n (c_{n-1} + 2 \cdot c_n + c_{n+1}) \cdot \varphi(t_{\max} + kT - nT)/2 = 0$$

Assume, for example, the above-described case of four dfe taps, where the four equations respectively correspond to k = 1, k = 2, k = 3 and k = 4. In this situation, Equation 7 would be evaluated for k = 1, k = 2, k = 3 and k = 4, thereby producing four separate equations. For each of the four values of k, the index n of Equation 7 takes the values of n = 1 and n = 2, thereby producing four filter taps c_0, c_1, c_2 and c_3.

Exemplary embodiments of a receiver DFE implementation according to the invention are shown in FIGURE 1. An analog AGC (automatic gain control) block buffers the analog input to prevent the feedback signal $s(t)$ from echoing back to the line. The buffered analog input signal $y(t)$, in this example current, is wire summed with the synthesized signal $s(t)$. The sampling receiver 13 takes samples from the mixed signal $z(t)$ to make the symbol decision. The decision symbols are then fed back to construct the new feedback signal $s(t)$. As shown in FIGURE 1, the decision symbols S_k (k = 1, … K) at different delay stages drive respective current source digital to analog converters (DAC) which are controlled by weights dfe_k (k = 1, … K) that define the taps of feedback signal $s(t)$.

In some embodiments, the tap weights dfe_k are real numbers in 2's complement format. Assuming, for example, that each weight dfe_k includes B bits which represent the magnitude of dfe_k, plus an additional bit to represent the sign of dfe_k, then for each of the K taps, the associated DAC has B parallel-connected current switch transistors. In some embodiments of FIGURE 1A, the B magnitude bits of dfe_k are thermometer-coded, and each of the resulting B thermometer-coded bits controls a respectively corresponding one of the B transistor switches. Each decision symbol S_k includes complementary bits s_k and $\overline{s_k}$ which are combined (e.g. multiplied) with the associated sign bit as shown in FIGURE 1A to control the polarity of the current that the corresponding DAC contributes to the wire summation node 15. Node 15 thus functions as a feedforward equalizer.

The receiver sampler and each delay stage are triggered by the symbol clock (not explicitly shown), so the $s(t)$ waveform is a square wave with each pulse having one-symbol duration T. The leading tap is time critical, so some embodiments require the circuit delay from the decision sampler 13 to the leading tap DAC output to be less than half of the symbol period.

Grounds for Rejection to be Reviewed on Appeal

Whether claims 1-4, 11, 12, and 23-25 are unpatentable under 35 USC 102(e) over U.S. Patent Application No. 2003/0058930.

Whether claims 13-16 are unpatentable under 35 USC 102(a) over U.S. Patent No. 6,469,988.

Whether claims 5-9 are unpatentable under 35 USC 103(a) over U.S. Patent Application No. 2003/0058930 and U.S. Patent No. 6,469,988.

Whether claim 10 is unpatentable under 35 USC 103(a) over U.S. Patent Application No. 2003/0058930 and U.S. Patent No. 7,027,499.

Whether claims 17-20 are unpatentable under 35 USC 103(a) over U.S. Patent Application No. 2003/0058930 and U.S. Patent No. 6,055,269.

Whether claim 21 is unpatentable under 35 USC 103(a) over U.S. Patent Application No. 2003/0058930, U.S. Patent No. 6,055,269, and U.S. Patent No. 6,678,105.

Whether claim 22 is unpatentable under 35 USC 103(a) over U.S. Patent Application No. 2003/0058930, U.S. Patent No. 6,055,269, and U.S. Patent No. 5,471,504.

Arguments

Rejection under 35 USC 102(a) as being unpatentable over U.S. Patent Application No. 2003/0058930

Claims 1-4, 11, 12, and 23-25

Claim 1 includes "...a feedforward equalizer coupled to said input for producing in response to said input analog communication signal an equalized analog communication signal ...". Claim 23 includes "…feedforward equalizing an input analog communication signal to produce an equalized analog communication signal …". U.S. Patent Application No. 2003/0058930 does not show, teach, or suggest the above recited limitations of claims 1 and 23. U.S. Patent Application No. 2003/0058930 does not disclose a feedforward equalizer for producing an equalized analog communication signal. The prefilter 12 in U.S. Patent Application No. 2003/0058930 is not an equalizer that produces an equalized analog communication signal.

Rejection under 35 USC 102(a) as being unpatentable over U.S. Patent No. 6,469,988.

Claims 13 and 16

Claim 13 includes "…said control information defined based on feedback coefficients used by a decision feedback equalizer in the communication receiver apparatus." U.S. Patent No. 6,469,988 does not show, teach, or suggest the above recited limitations of claim 13. U.S. Patent No. 6,469,988 does not disclose defining control information based on feedback coefficients used by a decision feedback equalizer. The filters in U.S. Patent No. 6,469,988 do not define control information based on feedback coefficients used by a decision feedback equalizer.

Rejection under 35 USC 103(a) as being unpatentable over U.S. Patent Application No. 2003/0058930 and U.S. Patent No. 6,469,988

Claims 5-9

Claims 5-9 depend from claim 1. Claim 1 includes "...a feedforward equalizer coupled to said input for producing in response to said input analog communication signal an equalized analog communication signal ...". U.S. Patent Application No. 2003/0058930 does not show, teach, or suggest the above recited limitations of claims 1 and 23. U.S. Patent Application No. 2003/0058930 does not disclose a feedforward equalizer for producing an equalized analog communication signal. The prefilter 12 in U.S. Patent Application No. 2003/0058930 is not an equalizer that produces an equalized analog communication signal.

Rejection under 35 USC 103(a) as being unpatentable over U.S. Patent Application No. 2003/0058930 and U.S. Patent No. 7,027,499

Claim 10

Claim 10 depends from claim 1. Claim 1 includes "...a feedforward equalizer coupled to said input for producing in response to said input analog communication signal an equalized analog communication signal ...". U.S. Patent Application No. 2003/0058930 does not show, teach, or suggest the above recited limitations of claims 1 and 23. U.S. Patent Application No. 2003/0058930 does not disclose a feedforward equalizer for producing an equalized analog communication signal. The prefilter 12 in U.S. Patent Application No. 2003/0058930 is not an equalizer that produces an equalized analog communication signal.

Rejection under 35 USC 103(a) as being unpatentable over U.S. Patent Application No. 2003/0058930 and U.S. Patent No. 6,055,269

Claims 17-20

Claim 17 includes "…an equalizer coupled between said input and said output for providing said equalized communication signal in response to said input communication signal, said equalizer having a control input for receiving an equalizer coefficient, said equalizer further responsive to said equalizer coefficient for producing said equalized communication signal …". U.S. Patent Application No. 2003/0058930 and U.S. Patent No. 6,055,269 do not show, teach, or suggest the above recited limitations of claim 17. U.S. Patent Application No. 2003/0058930 does not disclose an equalizer having a control input for receiving an equalizer coefficient and further responsive to said equalizer coefficient for producing said equalized communication signal. Feedback filter 16 in U.S. Patent Application No. 2003/0058930 is not an equalizer.

Rejection under 35 USC 103(a) as being unpatentable over U.S. Patent Application No. 2003/0058930, U.S. Patent No. 6,055,269, and U.S. Patent No. 6,678,105

Claim 21

Claim 21 depends from claim 17. Claim 17 includes "…an equalizer coupled between said input and said output for providing said equalized communication signal in response to said input communication signal, said equalizer having a control input for receiving an equalizer coefficient, said equalizer further responsive to said equalizer coefficient for producing said equalized communication signal …". U.S. Patent Application No. 2003/0058930 and U.S. Patent No. 6,055,269 do not show, teach, or suggest the above recited limitations of claim 17. U.S. Patent Application No. 2003/0058930 does not disclose an equalizer having a control input for receiving an equalizer coefficient and further responsive to said equalizer coefficient for

producing said equalized communication signal. Feedback filter 16 in U.S. Patent Application No. 2003/0058930 is not an equalizer.

Rejection under 35 USC 103(a) as being unpatentable over U.S. Patent Application No. 2003/0058930, U.S. Patent No. 6,055,269, and U.S. Patent No. 5,471,504

Claim 22

Claim 22 depends from claim 17. Claim 17 includes "…an equalizer coupled between said input and said output for providing said equalized communication signal in response to said input communication signal, said equalizer having a control input for receiving an equalizer coefficient, said equalizer further responsive to said equalizer coefficient for producing said equalized communication signal …". U.S. Patent Application No. 2003/0058930 and U.S. Patent No. 6,055,269 do not show, teach, or suggest the above recited limitations of claim 17. U.S. Patent Application No. 2003/0058930 does not disclose an equalizer having a control input for receiving an equalizer coefficient and further responsive to said equalizer coefficient for producing said equalized communication signal. Feedback filter 16 in U.S. Patent Application No. 2003/0058930 is not an equalizer.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-25 is improper, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejection.

To the extent necessary, the Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 20-0668 of Texas Instruments Inc.

Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,

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CLAIMS APPENDIX

1. A communication receiver apparatus, comprising:

an input for receiving from a communication transmitter apparatus an input analog communication signal;

a feedforward equalizer coupled to said input for producing in response to said input analog communication signal an equalized analog communication signal;

a sampler coupled to said feedforward equalizer for producing digital communication information in response to said equalized analog communication signal; and

a feedback equalizer coupled between said sampler and said feedforward equalizer for controlling said feedforward equalizer in response to said digital communication information.

2. The apparatus of Claim 1, wherein said feedforward equalizer includes a wire summation node.

3. The apparatus of Claim 1, wherein said feedback equalizer includes a digital-to-analog conversion portion having an input coupled to said sampler for receiving said digital communication information, said digital-to-analog conversion portion having an output coupled to said feedforward equalizer.

4. The apparatus of Claim 3, wherein said feedforward equalizer includes a wire summation node.

5. The apparatus of Claim 3, wherein said digital-to-analog conversion portion includes a plurality of digital-to-analog converters having respective inputs coupled to said sampler and having respective outputs coupled to said feedforward equalizer.

6. The apparatus of Claim 5, wherein each of said digital-to-analog converters includes a current source digital-to-analog converter.

7. The apparatus of Claim 6, wherein said outputs of said digital-to-analog converters are connected together at an input of said feedforward equalizer.

8. The apparatus of Claim 5, wherein said feedforward equalizer includes a wire summation node.

9. The apparatus of Claim 5, wherein said feedback equalizer includes a delay apparatus coupled between said sampler and said digital-to-analog converters for providing said digital communication information to said digital-to-analog converters at respectively different points in time.

10. The apparatus of Claim 1, wherein said input analog communication signal carries a SONET communication.

11. The apparatus of Claim 1, wherein said feedback equalizer includes a control input for receiving first control information, said feedback equalizer responsive to said control information for controlling said feedforward equalizer, said control information designed to minimize interference at temporal boundaries between data symbols carried by said equalized analog communication signal.

12. The apparatus of Claim 11, wherein said input analog communication signal is produced by the communication transmitter apparatus in response to second control information, said first control information designed in conjunction with the second control information to minimize interference at points in time between said temporal boundaries.

13. A communication transmitter apparatus, comprising:

an input for receiving digital communication information;

a digital-to-analog conversion portion coupled to said input for producing an analog communication signal in response to said digital communication information;

an output coupled to said digital-to-analog conversion portion for providing said analog communication signal for transmission to a communication receiver apparatus;

said digital-to-analog conversion portion having a control input for receiving control information, said digital-to-analog conversion portion for producing said analog communication signal in response to said control information, said control information defined based on feedback coefficients used by a decision feedback equalizer in the communication receiver apparatus.

14. The apparatus of Claim 13, wherein said digital-to-analog conversion portion includes a plurality of current source digital-to-analog converters, and wherein said control information includes weight information for indicating respective amounts of current to be sourced by said current source digital-to-analog converters.

15. The apparatus of Claim 13, wherein said control information is defined in conjunction with the feedback coefficients to minimize interference at points in time between temporal boundaries of data symbols carried by an equalized communication signal produced by the decision feedback equalizer.

16. The apparatus of Claim 15, wherein the feedback coefficients are defined in conjunction with said control information to minimize interference at said temporal boundaries.

17. A decision feedback equalizer apparatus, comprising:

an input for receiving an input communication signal;

an output for providing an equalized communication signal;

an equalizer coupled between said input and said output for providing said equalized communication signal in response to said input communication signal, said equalizer having a control input for receiving an equalizer coefficient, said equalizer further responsive to said equalizer coefficient for producing said equalized communication signal; and

a coefficient adaptor apparatus coupled to said equalizer for producing said equalizer coefficient, said coefficient adaptor apparatus having an input for receiving information

indicative of a temporal relationship between first and second points in time, said first point in time corresponding to an actual occurrence of a temporal boundary between data symbols carried by said equalized communication signal, said second point in time corresponding to an expected occurrence of said temporal boundary, and said coefficient adaptor apparatus for iteratively adapting said equalizer coefficient in response to said temporal relationship information.

18. The apparatus of Claim 17, wherein said temporal relationship information indicates when said first point in time precedes said second point in time, and also indicates when said second point in time precedes said first point in time.

19. The apparatus of Claim 17, wherein said coefficient adaptor apparatus includes logic for producing, in response to said temporal relationship information, equalizer information indicative of how said equalized communication signal is affected by a current version of said equalizer coefficient.

20. The apparatus of Claim 19, wherein said coefficient adaptor apparatus includes a coefficient adaptor coupled to said logic and having an input for receiving said current version of said equalizer coefficient, said coefficient adaptor responsive to said equalizer information for adapting said current version of said equalizer coefficient to produce a corresponding adapted version of said equalizer coefficient.

21. The apparatus of Claim 19, wherein said logic includes a lookup table.

22. The apparatus of Claim 17, wherein said coefficient adaptor apparatus is for implementing a LMS algorithm to iteratively adapt said equalizer coefficient.

23. A method of communication reception, comprising:

feedforward equalizing an input analog communication signal to produce an equalized analog communication signal;

producing digital communication information in response to said equalized analog communication signal; and

performing said feedforward equalizing step based on said digital communication information.

24. The method of Claim 23, including converting said digital communication information into an analog control signal, and performing said feedforward equalization step in response to said analog control signal.

25. The method of Claim 24, wherein said analog control signal is a current signal.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None